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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,058	08/09/2001	Kevin J. McGrath	5500-78200	4127

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,058	MCGRATH, KEVIN J.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/9/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because

in Fig. 12, inside Segment Registers (1054), between "CS" and "DS", --SS-- should be inserted; Similar problems exist in Figs. 13 and 14.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (U.S. Patent No. 5,721,855), herein referred to as Hinton et al.'855.

Referring to claim 1, Hinton et al.'855 discloses as claimed a processor (100, see Fig. 1) comprising: a register (RRFV field in RAT 138, see Fig. 18) configured to store a mask (the valid bits in RRFV field of RAT 138, see Fig. 18); and an execution core (the execution cores, such as IEU, FEU and MIU in Execution cluster 118, see Fig. 1) coupled to the register (RRFV field in RAT 138, see Fig. 18), wherein the execution core is configured, in response to a system call instruction (see Col. 30, lines 28-29, such as the logical micro-op (add EAX, EBX, EAX)), to selectively update each flag of a plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) responsive to a corresponding indication in the mask (the valid bits in RRFV field of RAT 138, see Fig. 18). Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at the corresponding entry RE36 is updated to 0 also.

Referring to claim 9, Hinton et al.'855 discloses as claimed an apparatus comprising: a storage location (RRFV field in RAT 138, see Fig. 18) configured to store a mask (the valid

bits in RRFV field of RAT 138, see Fig. 18); and a processor (100, see Fig. 1) coupled to the storage location (RRFV field in RAT 138, see Fig. 18), wherein the processor is configured, in response to a system call instruction (see Col. 30, lines 28-29, such as the logical micro-op (add EAX, EBX, EAX)), to selectively update each flag of a plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) responsive to a corresponding indication in the mask. Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at the corresponding entry RE36 is updated to 0 also.

Referring to claim 17, Hinton et al.'855 discloses as claimed a method comprising processing (by the processor 100, see Fig. 1) a system call instruction (see Col. 30, lines 28-29, such as the logical micro-op (add EAX, EBX, EAX)), the processing including selectively updating each flag of a plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) responsive to a corresponding indication in a mask (the valid bits in RRFV field of RAT 138, see Fig. 18). Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at the corresponding entry RE36 is updated to 0 also.

Referring to claim 22, Hinton et al.'855 discloses as claimed a processor (100, see Fig. 1) comprising: a register (RRFV field in RAT 138, see Fig. 18) configured to store a value (the valid value in RRFV field of RAT 138, see Fig. 18); and an execution core coupled to the register, wherein the execution core is configured, in response to a system call instruction (see Col. 30, lines 28-29, such as the logical micro-op (add EAX, EBX, EAX)), to selectively update each flag of a plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) responsive to the value (the valid value in RRFV field of RAT 138, see Fig. 18) in the register (RRFV field in RAT 138, see Fig. 18). Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at the corresponding entry RE36 is updated to 0 also.

As to claims 2, 10, and 18, Hinton et al.'855 also discloses: the execution core is configured to update a first flag of the plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) in response to the corresponding indication in the mask being in a first state (Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at

the corresponding entry RE36 is updated to 0 also) and wherein the execution core is configured to retain a current state of the first flag (see Fig. 22c, the flag V in entry RE36 of the ROB 136 is retained to "1") in response to the corresponding indication in the mask (see Fig. 22b, the mask RRFV in entry EAX of the RAT 132 is changed from "0" to "1") being in a second state (note when both the entry in ROB 136 and the corresponding entry in RAT 132 are valid is interpreted as in the second state).

As to claims 3, 11, and 19, Hinton et al.'855 also discloses: the execution core is configured to update the first flag by clearing the first flag (Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at entry EAX (ROB pointer 36) is changed from 1 to 0, then the flag (valid bit) at the corresponding entry RE36 is cleared to 0).

As to claims 4 and 12, Hinton et al.'855 also discloses: the corresponding indication is a bit (the mask bit in RRFV filed of RAT 132, see Fig. 18).

As to claims 5 and 13, Hinton et al.'855 also discloses: the first state comprises the bit being set (see Col. 30, line 56-58, regarding a set valid bit in ROB 136).

As to claims 6, 14, and 20 Hinton et al.'855 also discloses: the execution core (the execution cores, such as IEU,

FEU and MIU in Execution cluster 118, see Fig. 1) is coupled to receive an indication of an operating mode of the processor, and wherein the execution core is configured to selectively update each flag in the plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) in a first operating mode (the mode when the result data in the ROB 136 is speculative and the ROB 136 clears the valid flag such as that in the RE36 entry as shown in Fig. 18, see Col. 30, lines 65-67), and wherein the execution core is configured not to perform a selective update in a second operating mode (the mode when both the entry in ROB 136 and the corresponding entry in RAT 132 are valid is interpreted as in the second operating mode).

As to claims 7, 15, and 21, Hinton et al.'855 also discloses: the execution core is configured to perform a predetermined update (when the calculated result is sent to RS 138 and ROB 136, see Fig. 21b, the flag v at entry RE36 is updated) of the plurality of flags (valid V field of result buffer 1610 in ROB 136, see Fig. 18) in the second operating mode (the mode when both the entry in ROB 136 and the corresponding entry in RAT 132 are valid is interpreted as in the second operating mode). Note "a fixed update" in claim 21, line 1 is interpreted as "a predetermined update" as set forth in claim 7, line 2.

As to claims 8 and 16, Hinton et al.'855 also discloses: further comprising a second register (the V filed of RS 138, see Fig. 18) configured to store the plurality of flags (the valid bits in the V filed of RS 138, see Fig. 18), wherein the execution core is configured to store the updated plurality of flags in the second register (the V filed of RS 138, see Fig. 18) in response to the system call instruction (the inherent instruction to send the result to RS 138 and ROB 136 see Fig. 21b).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Diepstraten'468 also discloses a System for multitasking management employing context controller having event vector selection by priority encoding of context events. The event mask (321) and event status registers (320) are used. Jaggar et al.'358 discloses a system for executing multiple debug instructions. The control registers 20, 22 store control data such as mask values to be applied to the comparisons of the instruction bus IB and the data bus DB to the respective breakpoint and watchpoint values (see Col. 3, lines 58-68).

Griffth et al'263 discloses method and apparatus for partial and full stall handling in allocation. Each entry in the ROB 306 also contains fields for a instruction result (Pdst), a set of flags, a mask for the flags, a code that indicates what the results mean, and fault data (see col. 16, lines 45-48).

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

June 9, 2004